REMARKS

Claims 1-7 and 9-13 are pending in the present application. Claims 1, 3, 4 and 13 have been amended. Claim 14 has been canceled.

Claim Rejections-35 U.S.C. 103

Claims 1, 2, 5-7, 9-12 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Swoboda et al. reference (U.S. Patent No. 5,903,746) in view of Applicant's admitted prior art (AAPA). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The clock control circuit of claim 1 includes in combination among other features a high-speed clock source; a low-speed clock source; a selector; a first control section "that outputs the operation control signal for stopping the high-speed clock source responsive to a standy mode designated by a mode signal, that outputs the operation control signal for operating the high-speed clock source responsive to an interrupt signal, and that sets initial states of the central processing unit and causes the high-speed clock to be generated by the high-speed clock source a set time after a power source has been turned on, responsive to a reset signal"; and a second control section.

Applicant respectfully submits that the Swoboda et al. reference and Applicant's admitted prior art does not specifically disclose or suggest a first control section that sets initial states of a central processing unit and causes a high-speed clock to be generated a set time after a power source has been turned on, responsive to a reset

signal. Applicant therefore respectfully submits that the clock control circuit of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to the claims 1, 2, 5-7 and 9-12, is improper for at least these reasons.

Claim 5, as dependent upon claim 1, features that the selector includes in combination "a two-input OR gate, a two-input AND gate, a flip-flop having a reset input, a low-through latch, and an inverter". The Examiner has asserted that Fig. 8 and column 7, lines 15-24 of the Swoboda et al. reference disclose a selector including the above noted features.

Applicant however notes that Fig. 8 of the Swoboda et al. reference merely includes AND gates, OR gates, a NOR gate and inverters. Fig. 8 of the Swoboda et al. reference does not include a flip-flop having a reset input, or a low-through latch. Column 7, lines 15-24 of the Swoboda et al. reference as relied upon does not describe or even remotely suggest a flip-flop or a low-through latch. The Swoboda et al. reference therefore does not disclose the features of claim 5 as asserted by the Examiner. Applicant therefore respectfully submits that the clock control circuit of claim 5 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claim 5, is improper for at least these additional reasons.

With further regard to this rejection, the Examiner has asserted that Fig. 8 and column 7, lines 15-24 of the Swoboda et al. reference disclose the features of claim 11.

However, as asserted with respect to claim 5, these particular portions of the Swoboda et al. reference as specifically relied upon do not disclose or even remotely suggest a selector including a low-through latch. Applicant therefore respectfully submits that the clock control circuit of claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claim 11, is improper for at least these additional reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 3, 4 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant however respectfully submits that claims 3, 4 and 13 should be allowable at least by virtue of dependency upon claim 1, and that amendment of these claims to be in independent form is therefore unnecessary.

Applicant also emphasizes that claim 10 should be considered as including allowable subject matter by virtue of dependency upon claim 4. **The Examiner is therefore respectfully requested to acknowledge that claim 10 includes allowable subject matter.**

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the

corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to June 15, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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